BE Semester-VI EC Question Bank

VLSI Technology & Design

Each question carry 10 marks

Q.1. Derive current - voltage equation for NMOS.

Q.2 Explain n-well CMOS Process with necessary sketches.

Q.3 Explain following terms in short.

1) Body effect.
2) Moore's law
3) Threshold voltage.
4) Noise Margin
5) Channel length modulation

Q.4 Explain MOS system under external bias with necessary diagram.

Q.5 What is scaling? Why it is required? Explain full scaling.

Q.6 Explain MOS capacitance.

Q.7 For an n-channel MOS transistor $\mu_n = 700\ cm^2 / v.s$, $Cox = 8 .10^{-8}\ F/cm^2$ W= 20µm, L= 2 µm , $V_{TO} = 0.78V$. To calculate drain current at

(a) V_{GS} = 2v and V_{DS} = 1V
(b) V_{GS} = 3V and V_{DS} = 4V

Q.8. Draw CMOS and depletion NMOS load implementation for following Boolean equation

1) $Z = \overline{ADE + BC}$

2) $Z = \overline{A + DE + BC}$

Q.9. Draw CMOS implementation for following Boolean equation

$$Z = \overline{A(D + E) + BC}$$

Assume that (W/L)n = 10 for all nMOS and (W/L)p =15 for all pMOS. Find (W/L)equ for nMOS and pMOS.

Q.10. A CMOS inverter has $\mu_n c_{ox} = 120\ \mu A/ V^2$ $\mu_p c_{ox} = 60\ \mu A/ V^2$, $V_{TO,n} = 0.8$ V, $V_{TO,p} = -1.0$ V, $T_{PHL} = 0.2$ ns , $T_{PLH} = 0.15$ ns , V_{DD} = 3v C_{load} = 300 f f Determine (W/L)n and (W/L)p

Q.11 Explain voltage scaling. Explain effect of voltage scaling on drain current, power

dissipation and power density.

Q.12. Draw and explain working of CMOS inverter. Also Explain VTC of CMOS inverter.

Q.13 A CMOS inverter has $V_{TO,n}$ = 0.8 V, $V_{TO,p}$ = - 0.8 V , and $k_n=k_p$. Obtain $V_{IL,}$ V_{IH}, V_{OH},V_{OL} , NM_H and NM_L for V_{DD} = 5v .

Q. 14 Explain fabrication steps for nMOS with necessary figures.

Q.15. Draw and explain VTC of resistive load inverter.

Q.16 For an n- channel MOS X'tor with $\mu_n = 70\ cm^2/\ VS$, $c_{ox} = 8.\ 10^{-8}\ F/\ cm^2$,

$V_{TO,n}$ = 0.78 V, (W/L)n = 10 to calculate drain current for V_{GS} = 2V and V_{DS}= 4V.

Q.17 Write basic steps for NMOS fabrication steps. Explain LOCOS .

Q.18 Explain Substrate bias effect ,Punch through and hot electron effect.

Q.19 Draw and explain VTC of CMOS inverter. And explain Why (W/L)p = 2.5 (W/L)n.

Q.20 Design resistive Load inverter with resistor of value R_L = 50 KΩ , VDD = 12V, $V_{TO,n}$ = 4 V, Kn' = 25 µA/ V^2, $|2\Phi_F|$ = 0.6 V , V_{OL} = 0.5V .

Q.21 Explain different Limitations imposed by Small-Device Geometries for NMOS.

Q.22 Consider resistive load inverter circuit with VDD = 5V Kn' = 20 µA/ V^2 $V_{TO,n}$ = 0.8 V, R_L = 200 KΩ and W/L= 2 calculate noise margin of the circuit.

Q.23 Derive equation of T_{PLH} and T_{PHL} for CMOS inverter.

Q.24 Draw and explain SR and JK latch using CMOS implementation.

Q.25 Draw and explain NAND and NOR gate using CMOS implementation and depletion NMOS load implementation.

Q. 26 Draw and CMOS transmission gate.

Q. 27 Explain basic principal of pass transistor circuits. And also explain Voltage bootstrapping.

Q. 28 Draw and explain on chip clock generation and distribution.

Q.29 Explain Latch-up and also write its prevention.

Q. 30 Draw and explain CMOS D latch.

Q. 31 Explain Ad hoc testable design techniques.

Q.32 Draw and explain architecture of CPLD.

Q.33 Draw and explain architecture of FPGA.

Q.34 Explain PLD. Give difference between CPLD and FPGA.

Q.35 Explain controllability and observability. Also explain scan-based techniques.

Q.36 Explain built in self techniques.

Q. 37 Derive $V_{IL,}$ V_{IH}, V_{OH},V_{OL} for resistive load inverter.

Q. 38 Derive $V_{IL,}$ V_{IH}, V_{OH},V_{OL} for CMOS inverter.

Q. 39 Explain CMOS dynamic circuits techniques.

Q. 40 Explain different high performance dynamic CMOS circuits.